1. A method of forming shallow trench isolations in the fabrication of an integrated circuit device comprising:

growing a pad oxide layer overlying a silicon semiconductor substrate;

depositing a polysilicon layer overlying said pad oxide layer;

depositing a nitride layer overlying said polysilicon layer;

etching trenches through said nitride layer, said polysilicon layer, and said pad oxide layer into said silicon semiconductor substrate;

filling said trenches with an oxide layer wherein said oxide layer extends above a top surface of said nitride layer;

depositing a stop layer overlying said oxide layer;

first polishing away said stop layer and said oxide layer using a first slurry having high selectivity of oxide to nitride;

second polishing away said oxide layer using a second slurry having a low selectivity of oxide to nitride and having low-defect properties;

removing said nitride layer; and

thereafter third polishing away said oxide layer using a third slurry having a high selectivity of oxide to polysilicon to complete formation of said

shallow trench isolations in said fabrication of said integrated circuit device.

2. The method according to Claim 1 wherein said polysilicon layer has a thickness of between about 100 and 1000 Angstroms.

3. The method according to Claim 1 wherein said nitride layer comprises silicon nitride and has a thickness of between about 500 and 2000 Angstroms.

4. The method according to Claim 1 further comprising growing a liner oxide layer within said trenches before said step of depositing said oxide layer.

5. The method according to Claim 4 wherein said liner oxide layer and has a thickness of between about 50 and 300 Angstroms.

6. The method according to Claim 1 wherein said oxide layer is deposited by chemical vapor deposition.

7. The method according to Claim 1 wherein said oxide layer is deposited by high density plasma chemical vapor deposition.

8. The method according to Claim 1 wherein said stop layer is selected from the group consisting of: silicon oxynitride and silicon nitride and wherein said stop layer has a thickness of between about 50 and 1500 Angstroms.

9. The method according to Claim 1 wherein said first slurry has a selectivity of oxide to nitride of greater than 10.

10. The method according to Claim 1 wherein said second slurry has a selectivity of oxide to nitride of lower than 3.

11. The method according to Claim 1 wherein said second slurry uses silica-based particles to achieve said low-defect properties.

12. The method according to Claim 1 wherein said third slurry has a selectivity of oxide to polysilicon of greater than 10.

13. The method according to Claim 1 wherein said third polishing step uses a downforce of no more than half a conventional downforce.

14. A method of forming shallow trench isolations in the fabrication of an integrated circuit device comprising:

growing a pad oxide layer overlying a silicon semiconductor substrate;

depositing a polysilicon layer overlying said pad oxide layer;

depositing a nitride layer overlying said polysilicon layer;

etching trenches through said nitride layer, said polysilicon layer, and said pad oxide layer into said silicon semiconductor substrate;

filling said trenches with an oxide layer wherein said oxide layer extends above a top surface of said nitride layer;

depositing a silicon oxynitride layer overlying said oxide layer;

first polishing away said silicon oxynitride layer and said oxide layer using a first slurry having high selectivity of oxide to nitride;

second polishing away said oxide layer using a second slurry having a low selectivity of oxide to nitride and having low-defect properties;

removing said nitride layer; and

thereafter third polishing away said oxide layer using a third slurry having a high selectivity of oxide

to polysilicon to complete formation of said shallow trench isolations in said fabrication of said integrated circuit device.

15. The method according to Claim 14 wherein said polysilicon layer has a thickness of between about 100 and 1000 Angstroms.

16. The method according to Claim 14 wherein said nitride layer comprises silicon nitride and has a thickness of between about 500 and 2000 Angstroms.

17. The method according to Claim 14 further comprising growing a liner oxide layer within said trenches before said step of depositing said oxide layer.

18. The method according to Claim 17 wherein said liner oxide layer and has a thickness of between about 50 and 300 Angstroms.

19. The method according to Claim 14 wherein said oxide layer is deposited by one of the group consisting of: chemical vapor deposition and high density plasma chemical vapor deposition.

20. The method according to Claim 14 wherein said silicon oxynitride layer has a thickness of between about 50 and 1500 Angstroms.

21. The method according to Claim 14 wherein said first slurry has a selectivity of oxide to nitride of greater than 10.

22. The method according to Claim 14 wherein said second slurry has a selectivity of oxide to nitride of lower than 3 and wherein said second slurry uses silica-based particles.

23. The method according to Claim 14 wherein said third slurry has a selectivity of oxide to polysilicon of greater than 10.

24. The method according to Claim 14 wherein said third polishing step uses a downforce of no more than half a conventional downforce.

25. A method of forming shallow trench isolations in the fabrication of an integrated circuit device comprising:

growing a pad oxide layer overlying a silicon semiconductor substrate;

depositing a polysilicon layer overlying said pad oxide layer;

depositing a nitride layer overlying said polysilicon layer;

etching trenches through said nitride layer, said polysilicon layer, and said pad oxide layer into said silicon semiconductor substrate;

filling said trenches with an oxide layer wherein said oxide layer extends above a top surface of said nitride layer;

etching away said oxide layer except where it overlies said trenches; thereafter first polishing away said oxide layer and a portion of said nitride layer using a first slurry having low selectivity of oxide to nitride and having low-defect properties;

removing said nitride layers; and

thereafter second polishing away said oxide layer and a portion of said polysilicon layer using a second slurry having high selectivity of oxide to polysilicon to complete formation of said shallow trench isolations in said fabrication of said integrated circuit device.

26. The method according to Claim 25 wherein said polysilicon layer has a thickness of between about 100 and 1000 Angstroms.

27. The method according to Claim 25 wherein said nitride layer comprises silicon nitride and has a thickness of between about 500 and 2000 Angstroms.

28. The method according to Claim 25 further comprising growing a liner oxide layer within said trenches before said step of depositing said oxide layer wherein said liner oxide layer has a thickness of between about 50 and 300 Angstroms.

29. The method according to Claim 25 wherein said oxide layer is deposited by one of the group consisting of: chemical vapor deposition and high density plasma chemical vapor deposition.

30. The method according to Claim 25 wherein said first slurry has a selectivity of oxide to nitride of greater than 10.

31. The method according to Claim 25 wherein said second slurry has a selectivity of oxide to nitride of lower than 3.

32. The method according to Claim 25 wherein said second polishing step uses a downforce of no more than half a

conventional downforce.